

This application claims priority as a divisional to U.S. Patent Application
Serial No. 09/207,343 filed December 8, 1998.

IN THE CLAIMS:

Please cancel claims 1–15 without prejudice. Please amend the remaining claims as follows,
substituting any amended claim(s) for the corresponding pending claim(s):

- 1 16. (unchanged) A method for providing video motion compensation comprising the steps of:
- 2 receiving one or more prediction blocks;
- 3 receiving one or more instructions;
- 4 receiving one or more error terms; and
- 5 utilizing at least the one or more prediction blocks and the one or more error terms as directed
- 6 by the one or more instructions to produce a decoded macroblock.

1 17. (unchanged) A method for providing video motion compensation comprising the steps of:

2 receiving an instruction and writing the instruction to an instruction queue;

3 moving the instruction from the instruction queue to an execution unit if the execution unit
4 is not full;

5 receiving an error term and writing the error term to an error memory;

6 executing the instruction in the execution unit if the instruction is not a write instruction; and

7 if the instruction in the execution unit is a write instruction, waiting until the error memory
8 is full, and then utilizing at least all the error terms stored in the error memory and one or more
9 prediction blocks stored in a merge memory to produce a decoded macroblock.

1 18. (unchanged) The method for providing video motion compensation as recited in claim 17,

2 wherein the step of executing the instruction in the execution unit if the instruction is not a write

3 instruction further comprises the step of if the instruction in the execution unit is a load instruction,

4 reading a prediction block from a reference buffer, utilizing at least the prediction block and a half

5 pixel filter to produce a filtered prediction block, and writing the filtered prediction block to a merge

6 memory.

1 19. (unchanged) The method for providing video motion compensation as recited in claim 17,
2 wherein the step of executing the instruction in the execution unit if the instruction is not a write
3 instruction further comprises the step of if the instruction in the execution unit is a merge instruction,
4 reading a prediction block from a reference buffer, utilizing at least the prediction block and a half
5 pixel filter to produce a filtered prediction block, and merging the filtered prediction block with one
6 or more previously filtered prediction blocks.

1 20. (unchanged) A system for providing video motion compensation comprising:
2 a video decoder configured to produce one or more instructions and one or more error terms;
3 a picture memory; and
4 a digital video processor comprising an error memory communicably coupled to the video
5 decoder, a half pixel filter communicably coupled to the picture memory, a merge memory
6 communicably coupled to the half pixel filter, a controller communicably coupled to the video
7 decoder, the error memory, the merge memory and the half pixel filter, a sum unit communicably
8 coupled to the error memory, the merge memory and the picture memory, and the controller
9 executing the one or more instructions to provide motion compensation.

1 21. (unchanged) The system for providing video motion compensation as recited in claim 20, further
2 comprising:

- 3 an error buffer communicably coupled between the error memory and the video decoder;
- 4 an instruction buffer communicably coupled between the controller and the video decoder;
- 5 a reference buffer communicably coupled between the half pixel filter and the picture
- 6 memory; and
- 7 a display buffer communicably coupled between the sum unit and the picture memory.

1 22. (unchanged) The system for providing video motion compensation as recited in claim 21,
2 wherein the error memory, the merge memory, the picture memory, the error buffer, the instruction
3 buffer, the display buffer and the reference buffer are static random access memory.

Please add the following new claims:

1 23. (newly added) A digital video system comprising:

- 2 a DVD drive;
- 3 a track buffer communicably coupled to the DVD drive;
- 4 a demultiplexer communicably coupled to the track buffer
- 5 a video input buffer communicably coupled to the demultiplexer;
- 6 a digital video decoder communicably coupled to the video input buffer, the digital video
- 7 decoder utilizing at least an encoded video data stream to produce one or more output streams, the
- 8 one or more output streams comprising at least a set of motion compensation instructions and a set
- 9 of error terms;
- 10 a digital video processor coupled to the digital video decoder, the digital video processor
- 11 providing motion compensation using the set of motion compensation instructions and the set of
- 12 error terms;
- 13 a mixer communicably coupled to the digital video processor; and
- 14 a video renderer communicably coupled to the mixer.

1 24. (newly added) The digital video system as recited in claim 23, wherein the digital video
2 processor further comprises:

- 3 an error memory and a merge memory;
- 4 a half pixel filter communicably coupled to the merge memory;
- 5 a controller communicably coupled to the error memory, the merge memory and the half
6 pixel filter, the controller executing the motion compensation instructions; and
- 7 a sum unit communicably coupled to the error memory and the merge memory.

1 25. (newly added) The digital video system as recited in claim 24, wherein the digital video
2 processor further comprises:

- 3 an error buffer communicably coupled to the error memory;
- 4 an instruction buffer communicably coupled to the controller;
- 5 a reference buffer communicably coupled to the half pixel filter; and
- 6 a display buffer communicably coupled to the sum unit.

1 26. (newly added) The digital video system as recited in claim 24, wherein the controller further

2 comprises:

3 an instruction queue;

4 an execution unit communicably connected to the instruction queue and the error memory;

5 and

6 a motion compensation state machine communicably connected to the execution unit, the half
7 pixel filter and the merge memory.

1 27. (newly added) The digital video system as recited in claim 24, wherein the sum unit uses at least

2 one of the error terms stored in the error memory with one or more filtered prediction blocks stored

3 in the merge memory to produce a decoded macroblock.

1 28. (newly added) The digital video system as recited in claim 24, wherein the half pixel filter

2 performs vertical and horizontal half-pixel interpolation on a block as dictated by a motion vector.

1 29. (newly added) The method as recited in claim 16, further comprising:

2 receiving the one or more prediction blocks, the one or more instructions, and the one or

3 more error terms from a video decoder capable of selectively formulating the instructions.

1 30. (newly added) The method as recited in claim 16, further comprising:

2 filtering the one or more prediction blocks with a half pixel filter performing vertical and
3 horizontal half-pixel interpolation on each prediction block as dictated by a motion vector within an
4 instruction associated with the prediction block; and

5 utilizing each of the one or more error terms with an associated filtered prediction block from
6 the one or more prediction blocks filtered by the half pixel filter to produce the decode macroblock.

1 31. (newly added) The method as recited in claim 16, wherein the step of receiving one or more
2 instructions further comprises:

3 receiving at least one each motion compensation instruction comprising an instruction
4 descriptor followed by one or more data descriptors, the instruction descriptor comprising at least
5 a first data field and a second data field, the first data field indicating an operation to be performed
6 and the second data field indicating how many of the data descriptors follow the instruction
7 descriptor, each data descriptor comprising a third data field and a fourth data field, the third data
8 field indicating a memory address of a first word in a prediction block associated with the at least
9 one motion compensation instruction and the fourth data field indicating a number of words in the
10 prediction block.

1 32. (newly added) The method as recited in claim 16, further comprising:

2 utilizing the one or more instructions to control a motion compensation state machine
3 employed to produce the decoded macroblock.

1 33. (newly added) The method as recited in claim 16, further comprising:

2 storing the one or more received error terms within an error memory communicably coupled
3 to a controller for executing the one or more instructions.

1 34. (newly added) The method as recited in claim 16, further comprising:

2 filtering the one or more prediction blocks with a half pixel filter performing vertical and
3 horizontal half-pixel interpolation on each prediction block as dictated by a motion vector within an
4 instruction associated with the prediction block; and

5 storing filtered prediction blocks within a merge memory communicably coupled to a
6 controller for executing the one or more instructions.

1 35. (newly added) The method as recited in claim 16, further comprising:

2 storing the one or more instructions within an instruction queue communicably coupled to
3 a controller for executing the one or more instructions.